



Sheet	1	of	2
-------	---	----	---

Application Number	10/849,692
Filing Date	05/19/2004
First Named Inventor	Jared L. Zerger
Art Unit	2661
Examiner Name	Unknown
Attorney Docket Number	RA328.P.US

[illegible]

Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear
		Country Code <sup>3</sup> *Number*Kind Code <sup>2</sup> (if known)			
/DC/	4	EP 1 424 871 A2	02.06.2004	Alcatel Canada Inc.	
↓	5	WO 00/65791	02.11.2000	Graigh, John L.	
	6	EP 0 886 407 A2	23.12.1998	Hewlett-Packard Company	

08/09/2007

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

*If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.*



Approved for use through 07/31/2006. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Substitute for form 1449/PTO

(Use as many sheets as necessary)

Sheet	1	of	1
-------	---	----	---

**Complete if Known**

Application Number	10/849,692
--------------------	------------

Filing Date	05/19/2004
-------------	------------

First Named Inventor	Jared L. Zerbe
----------------------	----------------

Art Unit	2661
----------	------

Examiner Name	Unknown
---------------	---------

Attorney Docket Number	RA328.P.US
------------------------	------------

## U. S. PATENT DOCUMENTS

## FOREIGN PATENT DOCUMENTS

**Examiner  
Signature**

/Dady Chery/

Date  
Considered

08/09/2007

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

*If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.*

U.S. Department of Commerce, Patent and Trademark Office	Serial No.: Unknown
	Filing Date: May 19, 2004
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Inventor: Jared L. Zerbe
"Crosstalk Minimization in Serial Link Systems"	Group Art Unit: Unknown
	Examiner Name: Unknown
Express Mail No. ER 265640992 US	Attorney Docket No.: RA328.P.US

## U.S. Patent and U.S. Patent Publication Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
/DC/	A	6,396,887 B1	05/28/02	Ware et al.	375	354	
	B	6,366,991 B1	04/02/02	Manning	711	167	
	C	5,509,038	04/16/96	Wicki	375	371	
	D	6,661,863 B1	12/09/03	Toosky	375	376	
	E	6,504,438 B1	01/07/03	Chang et al.	331	17	
	F	US 2003/0053489 A1	03/20/03	Zerbe et al.	370	503	
	G	US 2003/0099190 A1	05/29/03	Zerbe	370	201	

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	H	JOHNSON, HOWARD DR., "Mitigating Crosstalk." High-Speed Digital Design - online newsletter - Vol. 6, Issue 01. January 20, 2003. Pages 1-3.
	I	"Shift Register Counters." Downloaded from <a href="http://www.eelab.usyd.edu.au/digital/tutorial/part/2/registor07.htm">http://www.eelab.usyd.edu.au/digital/tutorial/part/2/registor07.htm</a> . 09/17/02. 2 pages.
	J	STOJANOVIC, VLADIMIR et al., "Modeling and Analysis of High-Speed Links." Research supported by the MARCO Interconnect Focus Center and Rambus, Inc. September 2003. 8 pages.
	K	SIDIROPOULOS, STEFANOS et al., "Adaptive Bandwidth DLLs and PLLs Using Regulated Supply CMOS Buffers." 2000 Symposium of VLSI Circuits Digest of Technical Papers. 4 pages.
	L	SIDIROPOULOS, STEFANOS et al., "A Semidigital Dual Delay-Locked Loop." IEEE Journal of Solid-State Circuits, Vol. 32, No.11, November 1997. Pages 1683-1692.
	M	STOJANOVIC, VLADIMIR et al., "Adaptive Equalization and Data Recovery in a Dual-Model (PAM 2/4) Serial Link Transceiver." Rambus, Inc. Department of Electrical Engineering, Stanford University. January 2004. 4 pages.

Examiner

/Dady Chery/

Date Considered

08/09/2007

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

U.S. Department of Commerce, Patent and Trademark Office	Serial No.: Unknown
	Filing Date: May 19, 2004
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Inventor: Jared L. Zerbe
"Crosstalk Minimization in Serial Link Systems"	Group Art Unit: Unknown
	Examiner Name: Unknown
Express Mail No. ER 265640992 US	Attorney Docket No.: RA328.P.US

## U.S. Patent and U.S. Patent Publication Documents

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	N					
	O					
	P					
	Q					
	R					
	S					

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

/DC/	T	CHANG, KUN-YUNG KEN et al., "A 0.4-4Gb/s CMOS Quad Transceiver Cell Using On-Chip Regulated Dual-Loop PLLs." Rambus Inc., Los Altos, CA; T-RAM, San Jose, CA; Aeluros Inc, Mountain View, CA. May 2003. 4 pages.
	U	FARJAD-RAD, RAMIN, "A 0.4- $\mu$ m CMOS 10-Gb/s 4-PAM Pre-Emphasis Serial Link Transmitter." Center for Integrated Systems, Stanford University, Stanford, CA. May 1999. 2 pages.
	V	ZAND, BAHRAM et al., "High-Speed CMOS Analog Viterbi Detector for 4-PAM Partial Response Signalling." University of Toronto, Toronto, Canada. July 2002. 4 pages.
	W	ZERBE, J. et al., "Equalization and Clock Recovery for a 2.5 - 10 Gbs 2-PAM/4-PAM Backplane Transceiver Cell." Presented at ISSCC 2003, paper 4.6 2 pages.
	X	ZERBE, JARED L. et al., "Equalization and Clock Recovery for a 2.5-10-Gb/s 2-PAM/4-PAM Backplane Transceiver Cell." IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, December 2003. Pages 2121-2130.
	Y	

Examiner /Dady Chery/

Date Considered

08/09/2007

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.